

Search Text	
1	partition\$4 with (layout region design circuit)
2	(identif\$6 select\$4 determin\$4) near5 (region part\$4 portion section sub-\$7 net pin)
3	(partition\$4 with (layout region design circuit)) and ((identif\$6 select\$4 determin\$4) near5 (region part\$4 portion section sub-\$7 net pin))
4	(stor\$4 sav\$3 retriev\$4) with (rout\$4 wir\$4)
5	((partition\$4 with (layout region design circuit)) and ((identif\$6 select\$4 determin\$4) near5 (region part\$4 portion section sub-\$7 net pin))) and ((stor\$4 sav\$3 retriev\$4) with (rout\$4 wir\$4))
6	(generat\$4 creat\$4) with (rout\$4 wir\$4)
7	((partition\$4 with (layout region design circuit)) and ((identif\$6 select\$4 determin\$4) near5 (region part\$4 portion section sub-\$7 net pin))) and ((stor\$4 sav\$3 retriev\$4) with (rout\$4 wir\$4))) and ((generat\$4 creat\$4) with (rout\$4 wir\$4))
8	(stor\$4 sav\$3) with (rout\$4 wir\$4)
9	(retriev\$4) with (rout\$4 wir\$4)
10	((generat\$4 creat\$4) with (rout\$4 wir\$4)) and ((stor\$4 sav\$3) with (rout\$4 wir\$4)) and ((retriev\$4) with (rout\$4 wir\$4))
11	((partition\$4 with (layout region design circuit)) and ((identif\$6 select\$4 determin\$4) near5 (region part\$4 portion section sub-\$7 net pin))) and (((generat\$4 creat\$4) with (rout\$4 wir\$4)) and ((stor\$4 sav\$3) with (rout\$4 wir\$4)) and ((retriev\$4) with (rout\$4 wir\$4))))

	Search Text
1	716/7.ccls.
2	716/8.ccls.
3	716/9.ccls.
4	716/10.ccls.
5	716/11.ccls.
6	716/12.ccls.
7	716/13.ccls.
8	716/14.ccls.
9	716/15.ccls.
10	716/16.ccls.
11	716/17.ccls.
12	716/18.ccls.

	Search Text
1	716/1.ccls.
2	716/2.ccls.
3	716/3.ccls.
4	716/4.ccls.
5	716/5.ccls.
6	716/6.ccls.